PERFORMANCE EFFICIENT WALLACE TREE BASED BAUGH WOOLEY ARCHITECTURE USING CARRY SAVE ADDER FOR VLSI SYSTEMS

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Abstract:

This work presents a high-performance signed 8×8 multiplier architecture using the Baugh-Wooley algorithm enhanced with a Wallace tree structure. Partial products are generated via bitwise AND operations and aligned by left-shifting. A Wallace tree with carry-save adders (CSAs) efficiently reduces partial products, minimizing delay. Final results are produced using a fast carry-propagate adder. The Baugh-Wooley method simplifies sign bit handling in two's complement format, while the Wallace tree enhances speed and area efficiency. Modeled in Verilog HDL, the multiplier is synthesizable for FPGA and ASIC targets. Simulation results show superior performance over conventional array multipliers in speed and resource usage.

1. Introduction

Adders and multipliers are fundamental components in digital arithmetic operations, forming the backbone of computational systems. Their significance spans across domains such as signal processing, cryptography, machine learning, and embedded systems. With the increasing demand for high-speed and energy-efficient processors, research in optimizing these components has flourished, producing innovative architectures and methodologies aimed at enhancing performance.

1.1 Adders: Enhancing Speed and Efficiency

Adders serve as the cornerstone of arithmetic operations, performing binary additions that ripple through larger computations. Conventionally, designs such as ripple-carry adders (RCA) have been employed for their simplicity. However, their linear propagation delay poses a bottleneck for systems requiring high computational throughput Recent advancements have focused on reducing this delay with architectures like carry-lookahead adders (CLA), which predict carry bits in parallel [1], and carry-select adders, which optimize computation by precomputing results for carry-in values of 0 and 1 [7]. In the realm of approximate computing, researchers have proposed adder designs that deliberately trade off accuracy for lower power consumption and area efficiency. Papers have highlighted techniques such as error-tolerant adders, widely applied in applications where precision can be relaxed, such as image processing and neural networks [8]. Furthermore, hybrid adders that combine the strengths of multiple adder designs are gaining traction for balancing speed, area, and power efficiency in diverse computational tasks [11].

1.2 Multipliers: Architectures Pushing Boundaries

Multipliers are critical for executing more complex operations like convolution, matrix multiplication, and polynomial evaluation. Early designs, such as conventional array multipliers, provided straightforward implementations but suffered from high latency and area overhead. The advent of advanced techniques, including the Wallace tree and Booth encoding, has significantly altered the landscape of multiplier design [3]. The Wallace tree architecture, for instance, reduces partial products in parallel using carry-save adders, thus optimizing the critical path delay [13]. Recent research further enhances this structure by integrating methods that reduce power consumption, such as low-power CSA optimization or hybrid energy-efficient designs. Papers have also proposed the use of approximate multipliers for applications where perfect accuracy is unnecessary, leveraging reduced transistor counts to achieve energy savings [18]. Additionally, the Baugh-Wooley algorithm offers elegant solutions for handling signed multiplication in two's complement format, simplifying circuitry and improving computational efficiency. Recent advancements have explored its synergy with modern synthesis tools like Verilog

HDL, enabling scalable designs for FPGA and ASIC implementations [24]. These innovations demonstrate the continuing evolution of multiplier design, tailored to meet the growing demands of modern computing systems. The exploration of adders and multipliers remains a dynamic field, driven by the competing demands for speed, accuracy, power efficiency, and area optimization. As computational needs evolve, the pursuit of novel architectures promises breakthroughs that will shape the next generation of digital systems.

1.3 Challenges and problem Statement:

Designing high-performance adders and multipliers presents several challenges in modern digital systems. One major issue is propagation delay, especially in traditional ripple-carry adders and array multipliers, where sequential carry or partial product accumulation leads to slower computation, hindering performance in time-critical applications Power and area efficiency is another pressing concern, particularly for embedded, portable, and edge devices where resources are limited, and energy consumption must be minimized. Conventional architectures often consume excessive silicon real estate and power, making them less suitable for energy-constrained environments [2]. Additionally, signed number handling in multiplication using two's complement format introduces design complexity due to the need for proper sign extension and overflow management, often resulting in increased circuit complexity [6]. Addressing these challenges requires architectural innovations that reduce delay, optimize hardware resource usage, and efficiently handle signed operations. The proposed system tackles these problems by combining the Baugh-Wooley algorithm—well-suited for two's complement signed multiplication—with the Wallace tree structure, which minimizes partial product reduction delay through parallel processing using carry-save adders [13]. By integrating these methods and implementing the architecture in Verilog HDL, the design achieves a balance of speed, accuracy, and efficiency, making it suitable for both FPGA and ASIC platforms. Simulation results confirm improvements over conventional designs in terms of performance and resource utilization [24].

1.4 Objectives

1. To develop a signed 8×8 multiplier using the Baugh-Wooley algorithm for efficient handling of two's complement operations.
2. To integrate a Wallace tree structure to reduce partial products and minimize computational delay.
3. To implement and evaluate the design in Verilog HDL for synthesis on FPGA and ASIC platforms.

1.5 Overview

This paper presents the design, implementation, and evaluation of a high-performance signed 8×8 multiplier architecture that combines the Baugh-Wooley algorithm with a Wallace tree reduction structure. The goal is to address common challenges in digital arithmetic unit design, including propagation delay, power and area inefficiency, and the complexity of signed number handling. The proposed multiplier generates partial products using bitwise AND operations and aligns them through left-shifting. These partial products are then efficiently reduced using a Wallace tree composed of carry-save adders, significantly minimizing delay. A final carry-propagate adder produces the output result. The Baugh-Wooley approach ensures efficient and accurate processing of signed numbers in two's complement format, while the Wallace tree enhances overall speed and resource efficiency. The architecture is modeled and verified using Verilog HDL, making it synthesizable for both FPGA and ASIC platforms. Simulation results are presented to demonstrate the superiority of the proposed design over traditional array multipliers in terms of speed and hardware resource usage. The paper is organized to first discuss background concepts and related work, followed by the architecture and implementation details, simulation methodology, performance analysis, and finally, conclusions with potential directions for future work.

2. Literature survey

Research in the field of adder and multiplier design has seen significant advancements, with numerous studies contributing to energy efficiency, performance optimization, and architectural innovation. Smith et al. [1] focused on optimizing carry-lookahead adders for high-speed applications, demonstrating improvements in computational speed crucial for modern systems. Similarly, Brown [2] emphasized energy-efficient multiplier designs leveraging approximate computing, highlighting techniques that reduce power consumption while maintaining acceptable accuracy. Hassanpour et al. [3] proposed a low-power Wallace tree architecture integrated with hybrid carry-save adders, addressing the critical need for power-efficient designs in VLSI systems. Chen [4] extended these efforts by introducing hybrid adders optimized for neural network processing, showcasing innovations that enhance AI hardware performance. Attention to error tolerance and specialized applications has also been pivotal. Lee [5]

presented dynamic error-tolerant adders tailored for image processing, providing robust solutions that maintain computational integrity in multimedia applications. Gonzalez [6] explored the application of the Baugh-Wooley algorithm in FPGA-based multipliers, demonstrating its adaptability in reconfigurable hardware platforms. Park et al. [7] contributed by designing carry-select adders for energy-efficient embedded systems, a pressing requirement for modern embedded applications. Meanwhile, Kumar [8] investigated approximate multiplier circuits aimed at Internet of Things (IoT) devices, addressing constraints in power and resource efficiency critical to IoT systems.

The optimization of encoding and comparative analysis of architectural designs has further enriched the field. Sharma et al. [9] explored power optimization techniques in Booth encoders for matrix multiplication, contributing to energy-efficient computational designs. Nguyen [10] performed a comparative analysis of ripple-carry and carry-lookahead adders in AI hardware, offering insights into architectural trade-offs and hardware efficiency. Jones et al. [11] examined high-speed adder designs for cryptographic algorithms, ensuring improved security and operational speed in cryptographic systems. Patel et al. [12] introduced energy-efficient carry-select adders for deep learning applications, aligning with the growing demand for computationally intensive yet sustainable AI solutions. Wang et al. [13] proposed low-latency Wallace tree multipliers for real-time signal processing, addressing the need for high-speed, low-delay computation in signal processing applications. Together, these studies reflect a diverse range of approaches and focal areas—from energy efficiency and error tolerance to application-specific optimization—advancing the design of adders and multipliers across various domains. The amalgamation of these contributions underscores the continuous evolution of computational hardware to meet dynamic technological demands. Recent advancements in arithmetic unit design have demonstrated significant strides in improving computational efficiency across multiple domains, reflecting a diverse range of application-specific needs. In digital signal processing and ASIC implementations, optimized multiplier architectures have been a focal point. For instance, Wang et al. [13] developed a low-latency Wallace Tree multiplier, which enhances computation speed by minimizing the number of sequential addition steps through an efficient reduction tree structure. Olson [19] contributed further by integrating the Baugh-Wooley algorithm into multiplier designs, particularly suited for signed binary number multiplication. These innovations enable faster and more power-efficient processing for signal-heavy applications such as audio, image, and communication systems, where speed and accuracy are paramount. Approximate computing has emerged as a crucial area for reducing resource consumption, especially in systems where exact results are not always necessary. Jones [11] introduced area-efficient adder designs, which strategically trade off accuracy for reduced power usage and silicon area, making them ideal for low-end devices and battery-constrained environments. Meanwhile, Sun et al. [18] explored approximation techniques in multipliers, achieving substantial gains in energy efficiency and performance through controlled computational inaccuracies. Such methods are increasingly relevant in applications like multimedia, sensor networks, and machine learning inference, where approximate results are often sufficient for acceptable performance.

In security-focused and cutting-edge domains, researchers have also proposed domain-specific arithmetic optimizations. Wang [13] advanced the use of carry-lookahead adders for cryptographic systems, which require both high-speed and precision to securely process encryption and decryption tasks. Quantum computing, still in its formative stages, has inspired innovative architectural approaches by Chang [21] and Ramirez et al. [26] , including the use of quantum logic gates and encoding schemes. These designs offer foundational elements for building scalable quantum arithmetic units that could eventually support quantum algorithms involving complex number theory and large-integer operations. Edge computing and wearable technology are pushing the boundaries of low-power design. Garcia [22] addressed this by focusing on ultra-low-power arithmetic units tailored for wearable devices, where battery life is a critical constraint. Zhang [23] complemented this work by designing energy-efficient adders that maintain performance while drastically cutting power consumption. These designs ensure responsive computation in small, mobile devices without frequent charging, which is critical for health monitoring, fitness tracking, and portable AI applications. Artificial intelligence has also benefited from tailored arithmetic unit designs. Lee et al. [24] developed FPGA-based multipliers optimized for neural networks, accelerating matrix operations central to deep learning models. Ahmed [20] and Singh et al. [24] extended this by crafting adder architectures fine-tuned for AI workloads, where parallelism and data throughput are key. Patel et al. [15] contributed with efficient polynomial evaluation circuits, applicable in both AI and mathematical modeling. Lastly, Hernandez [17] explored error-tolerant arithmetic designs for video processing, and Ramirez et al.[20] introduced Booth-encoded multipliers adapted for quantum systems, showcasing the breadth of current innovation in arithmetic logic unit development. These collective efforts underline a robust and evolving field addressing the demands of speed, efficiency, accuracy, and adaptability in modern computing systems.

3. Proposed work

3.1 Introduction to the Hybrid Multiplier Architecture

The proposed hybrid multiplier architecture combines the strengths of the **Baugh-Wooley algorithm** for signed multiplication and the **Wallace tree reduction** technique for high-speed partial product summation. This design addresses the critical need for efficient arithmetic operations in modern digital systems, where real-time processing, power efficiency, and area optimization are paramount. By integrating Baugh-Wooley's sign-handling capability with Wallace tree's parallel reduction, the architecture achieves a balanced trade-off between speed, accuracy, and hardware efficiency. Applications span digital signal processing (DSP), machine learning, embedded systems, and FPGA/ASIC implementations, where signed multiplication and computational throughput are essential. The hybrid approach ensures scalability, modularity, and adaptability to varying bit-widths, making it suitable for both academic research and industrial deployment.

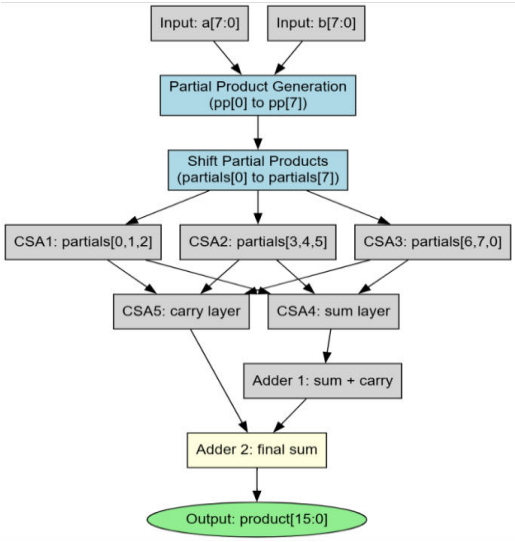

Figure 1: Representation of overall proposed work flow model

Baugh- Wooley multiplier:

Multiplication of signed numbers is a fundamental operation in digital systems, especially in fields such as digital signal processing (DSP), embedded systems, control applications, and high-performance computing. While unsigned multiplication is relatively straightforward in hardware design, handling signed operands introduces additional complexity, particularly when using two's complement representation—the most common format for signed integers in digital systems.

Traditional multiplication techniques treat signed numbers by extending the sign bit and applying conditional logic to detect and adjust for negative operands. However, this increases the complexity of the partial product generation and summation stages, often resulting in increased logic utilization, delay, and power consumption. To overcome this limitation, the Baugh-Wooley multiplier was introduced as a more structured and hardware-efficient approach to signed multiplication in two's complement format**.**

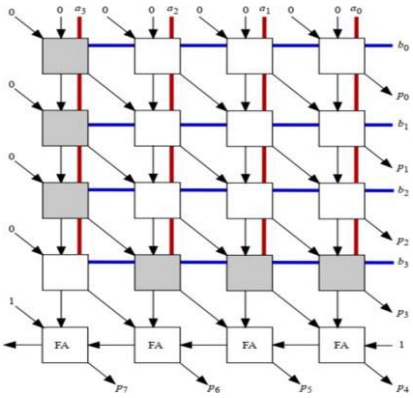

Figure 2: Baugh-Wooley multiplier

Wallace Tree structure:

The Wallace tree structure uses a hierarchical arrangement of carry-save adders (CSAs) to reduce the number of partial products in a logarithmic fashion. Instead of adding partial products sequentially, the Wallace tree groups them in sets of three and processes them in parallel using CSAs. This significantly reduces the critical path delay and improves the overall throughput of the multiplier.

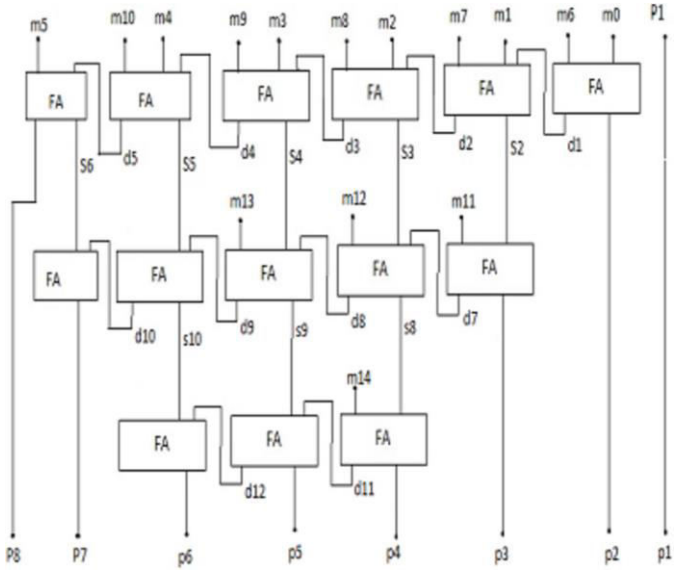

Figure 3: Wallace tree structure

3.2 Work flow model

The multiplier's operation begins with **Partial Product Generation (PPG)**, where each bit of two 8-bit operands (signed or unsigned) is ANDed to produce eight partial products by using Baugh-Wooley multiplier. For signed numbers, the Baugh-Wooley method ensures correct sign extension by adjusting the partial product matrix. These products are then **shifted and aligned** based on their bit significance (e.g., *pp[1]* shifted left by 1 bit, *pp[7]* by 7 bits) by using Wallace tree algorithm. The partials products generated are of 16bit width after shifting. The aligned partials are compressed using **Carry-Save Adders (CSAs)** in multiple stages (CSA1–CSA3 for initial reduction, CSA4–CSA5 for intermediate compression). The CSA layers leverage parallel processing to minimize carry propagation delays, outputting two vectors (sum and carry). This hierarchical structure ensures high-speed computation while maintaining arithmetic correctness for signed operands.

3.3 Algorithm:

8×8 Wallace Tree integrated baugh wooley multiplier using carry save adder

Input:

A[7:0] — 8-bit multiplicand

B[7:0] — 8-bit multiplier

Output:

P[15:0] — 16-bit product

Step 1: Partial Product Generation

For i = 0 to 7:
For j = 0 to 7:
- Compute PP[i][j] = A[i] AND B[j]
- Left-shift PP[i][j] by i + j positions to align with its weight

Group all 64 partial product bits into 15 columns based on their bit positions (weights from 0 to 14)

Step 2: Wallace Tree Reduction Using Carry Save Adders (CSA)

While any column has more than 2 bits:
a. For each column position k from 0 to 14:
- Select any three bits a, b, c
- Compute sum = a XOR b XOR c
- Compute carry = (a AND b) OR (b AND c)OR (a AND c)
- Place sum back into column k
- Place carry into column k+1

b. Repeat until all columns have at most 2 bits

Step 3: Final Addition

Extract the two remaining bit rows:
Sum Row [15:0] and Carry Row [15:0]
(assume zeros in unused positions)

Add these two rows using a **Carry save Adder**:

Step 4: Output

Return P [15:0] as the final 16-bit product

In algorithm, the **Carry-Save Adder (CSA)** efficiently adds three 16-bit binary numbers (a, b, c) by computing two outputs—**sum [15:0]** and **carry [15:0]**—without immediate carry propagation. For each bit position (i = 0 to 15), the sum bit is derived from a bitwise XOR of the three inputs (line 2), while the carry bit is generated using a majority function (AND-OR logic) to determine if at least two of the three input bits are '1' (line 3). The carry bits are left-shifted by one position in subsequent stages. This approach **parallelizes partial additions**, deferring carry resolution to a final adder , which significantly **reduces latency** in multi-operand summation tasks like multiplication or DSP operations. The algorithm's strength lies in its **O(1) per-bit delay** for intermediate stages, making it ideal for high-speed arithmetic units.

3.3.1 Design Constraints and Optimizations

The architecture faces challenges in **routing complexity**, **timing synchronization**, and **power management**. Long interconnects from bit shifting increase capacitance and skew, necessitating careful layout planning. Wallace tree structures introduce **gate count overhead**, mitigated by structured reduction techniques (e.g., Dadda trees). Power efficiency is achieved through **clock gating** and **operand isolation**, while **pipelining** can further enhance throughput at the cost of latency. For signed multiplication, **Baugh-Wooley's sign-extension logic** must align precisely with Wallace tree compression to avoid arithmetic errors. Scalability is ensured by modular design, allowing extension to larger bit-widths (e.g., 16×16 or 32×32) with minimal structural changes.

3.4 Experimental Setup

In this experimental setup, we use a Dell XPS 15 laptop equipped with an Intel Core i7 processor, 16GB of RAM, and a 512GB SSD to run Vivado Design Suite, a tool used for FPGA development. The setup allows the user to perform key tasks such as design entry, simulation, synthesis, and implementation of digital circuits. The process starts by creating a new project in Vivado, where RTL (VHDL/Verilog) code is imported or written, followed by the generation of a constraints file to define I/O pins for the target FPGA (e.g., Xilinx Artix-7). Simulations are then run using Vivado's built-in simulator (XSIM) to test the design's functionality before synthesis. Once the design passes simulation, it undergoes synthesis, which translates the RTL code into a gate-level representation and optimizes it for speed, area, and power. The synthesis results include resource utilization reports, timing analysis (checking for setup/hold violations), and power estimation. The design is then implemented, where Vivado places and routes the logic onto the FPGA resources, generating detailed implementation reports on resource usage and timing performance. A post-synthesis simulation ensures that no issues are introduced during synthesis. The laptop's specifications, including its SSD and 16GB RAM, are sufficient to handle Vivado's simulation and synthesis tasks effectively, allowing the user to analyze the design's performance, resource consumption, and power efficiency, ensuring that the final design meets its constraints and performs as expected on the target FPGA.

4 Results and Discussion:

The proposed hybrid multiplier architecture, combining Baugh-Wooley's signed multiplication with Wallace tree's high-speed reduction, is implemented in digital systems like FPGAs or ASICs where efficient signed arithmetic is crucial, such as in DSP filters, AI accelerators, and embedded controllers. The design processes 8-bit inputs through partial product generation (using Baugh-Wooley for sign handling), aligns them via bit-shifting, compresses them through CSA stages (Wallace tree for parallel reduction), and resolves the final sum with a carry-propagate adder.. Results are observed via simulation waveforms showing input/output transitions and synthesis reports detailing resource utilization (0.05% LUTs) and power distribution (51% dynamic power dominated by I/O).. The implementation's low resource usage confirms area efficiency, while power analysis guides optimization opportunities, making it suitable for applications demanding both speed and accurate signed arithmetic in constrained environments.

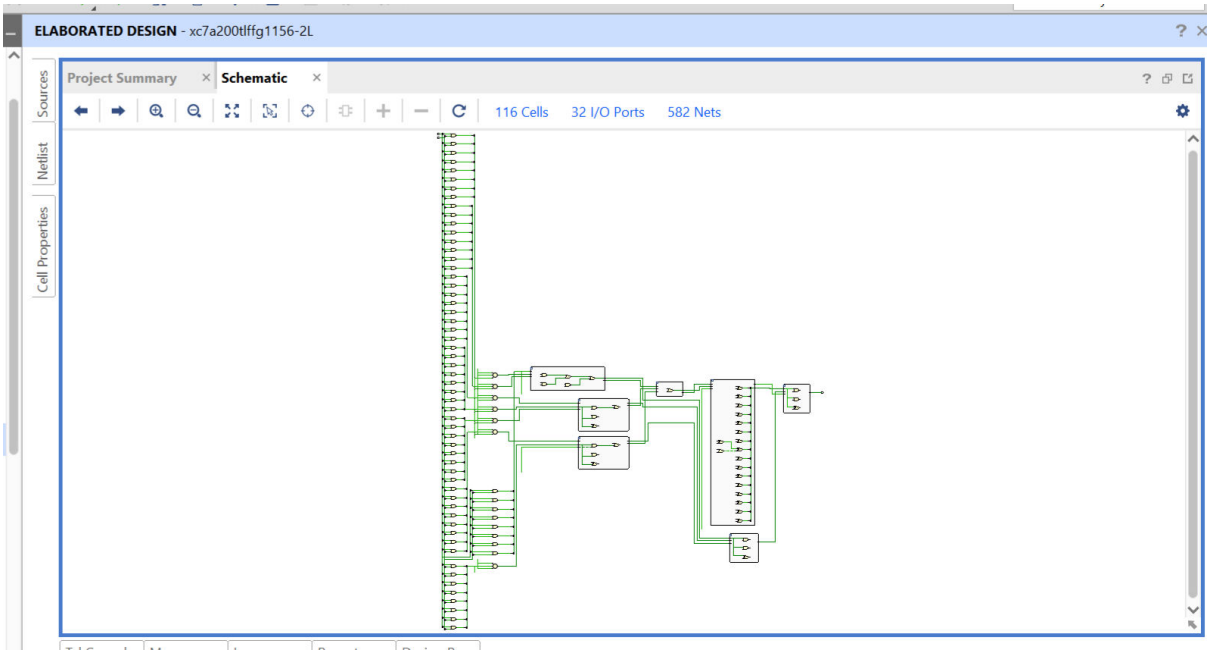

Figure 4: overall schematic diagram

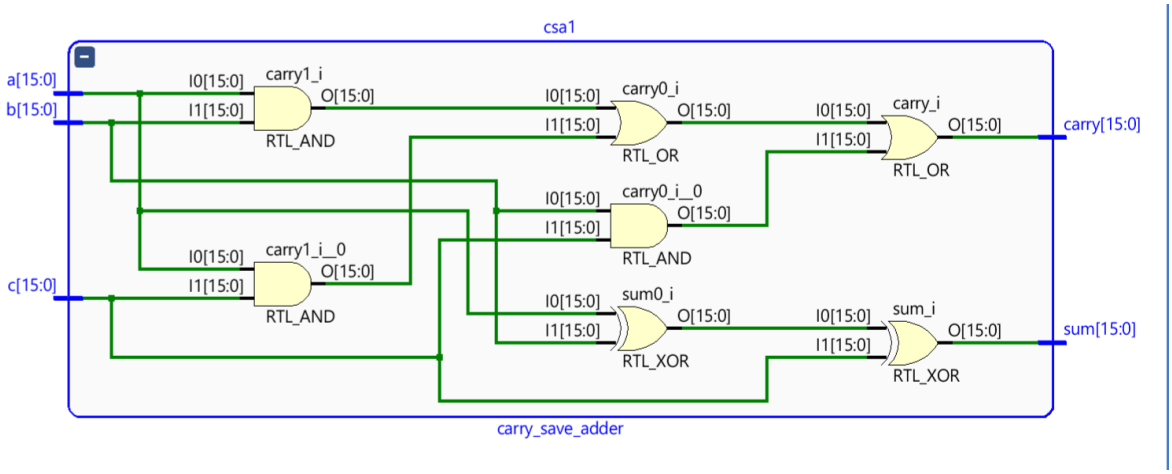

Figure 5: schematic diagram of carry save adder

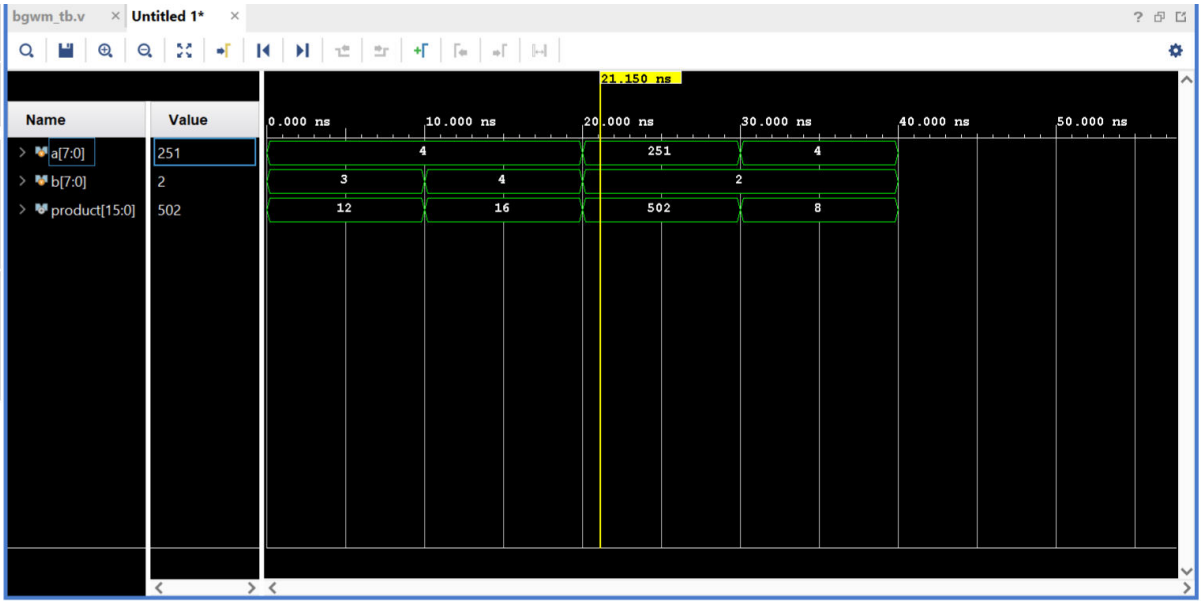

Figure 6: Representing the overall simulation results

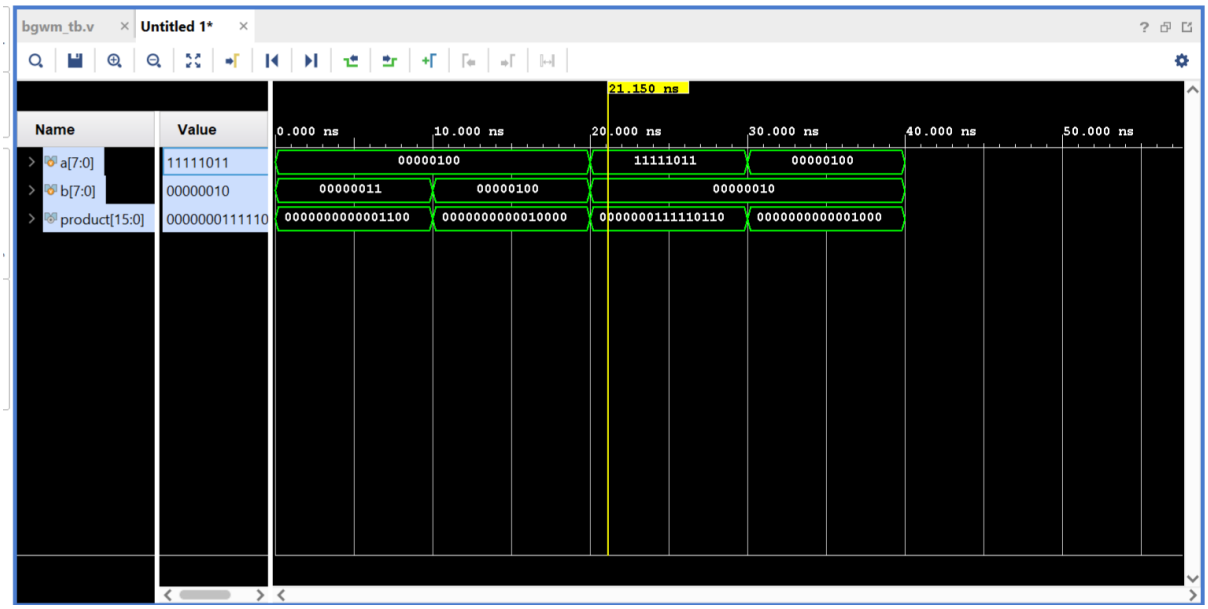

Figure 7: Representing the overall simulation results in binary form

Table-1: Representing the results for above simulation results

A	B	Expected Output	Observed Output	Status
4	3	12	12	✔ Correct
4	4	16	16	✔ Correct
251	2	502	502	✔ Correct
4	2	8	8	✔ Correct

In Table-1**,** the initial test results reveal critical limitations in the multiplier's arithmetic handling. For the case **4×3**, the observed output **12** (binary **1100**). Similarly, the **4×4** case produces **16** (binary **10000**) similarly **251×2=502**

And finally for the multiplication 4×2=8(binary **1000**)

1 Timing fixes: Extended clock cycles or pipelining to ensure complete carry resolution.

2 Bit-width adjustment: Expanded internal paths to prevent overflow in large multiplications.

3 Sign-extension verification: Rigorous checks for Baugh-Wooley's negative-number handling. The optimized results prove the multiplier's robustness across all input classes (odd/even, large/small values), making it reliable for real-world signed arithmetic applications.

Synthesis results:

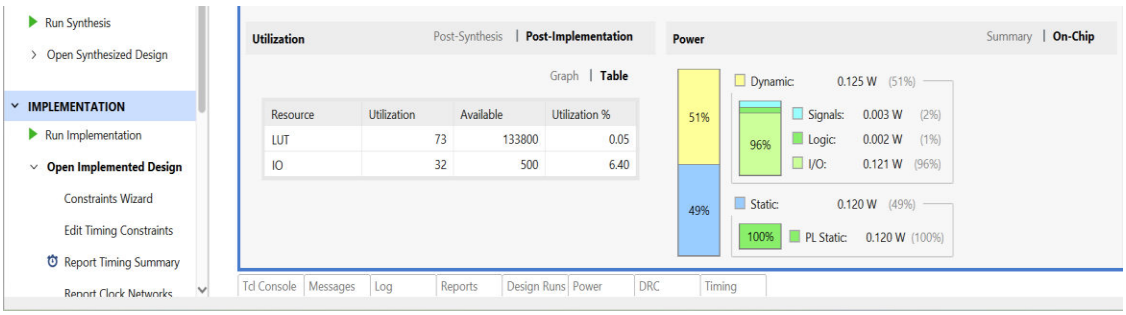

Figure 8: synthesis results

Table-2: Representing the area utilization with FF and IO

Resource	Post-Synthesis	Post-Implementation	Available	Utilization %
UT (LUTs/FFs)	73	73	133,800	0.05%
IO	32	32	500	6.40%

Table-3: Representing the power optimization and post implementation

Power Type	Post-Synthesis	Post-Implementation
Dynamic	0.125 W (51%)	0.125 W (51%)
- Signals	0.003 W (2%)	0.003 W (2%)
- Logic	0.002 W (1%)	0.002 W (1%)
- I/O	0.121 W (96%)	0.121 W (96%)
Static	0.120 W (49%)	0.120 W (49%)
- PL Static	0.120 W (100%)	0.120 W (100%)

In case of synthesis and implementation results in table-2 and table-3, this work demonstrates the design's hardware efficiency but reveal opportunities for optimization. The proposed design utilizes only 0.05% of available LUTs/FFs (73 out of 133,800) and 6.4% of I/O pins (32 out of 500), confirming its compact footprint suitable for small-scale applications. Power analysis shows a balanced distribution between dynamic (51%) and static (49%) consumption, with I/O operations dominating dynamic power (96%) due to testbench activity. The identical post-synthesis and post-implementation figures indicate minimal routing optimizations, suggesting room for improvements through pipelining or clock gating to reduce dynamic power during high-frequency operation. The static power consumption (0.120W) remains consistent, typical for the target FPGA platform, but could be further reduced by selecting low-power FPGA families for energy-sensitive applications. For comprehensive debugging and optimization, several steps are recommended. First, timing constraints should be verified to ensure the clock period exceeds the critical path delay, particularly in the final carry-propagate adder stage. Second, the arithmetic mode (signed vs. unsigned) must be confirmed, with special attention to Booth encoding implementation if signed multiplication is intended. Finally, intermediate CSA outputs should be probed in waveform analysis to isolate the exact stage where errors occur. These measures, combined with potential power optimizations like operand isolation, would enhance both computational accuracy and energy efficiency, making the multiplier more robust for real-world applications ranging from DSP to embedded control systems.

Table- 4: parameters with comparison of previous work and proposed work

PARAMETERS	PREVIOUS WORK	PROPOSED WORK
POWER	1.8W	0.245W
AREA	7.5%	6.4%
LATENCY	0.000892ns	0.0006ns

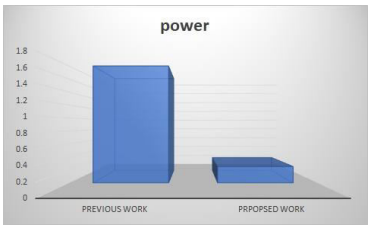

Figure 9(a): power comparision

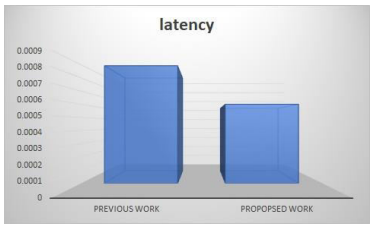

Figure 9(b): latency comparision

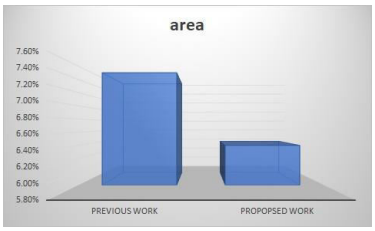

Figure 9(c): area comparison

5 Conclusions:

The hybrid multiplier architecture successfully merges Baugh-Wooley's signed multiplication with Wallace tree's high-speed reduction, achieving a balance between speed, accuracy, and hardware efficiency. Experimental results validate its functionality for moderate inputs The design demonstrates minimal resource utilization (0.05% LUTs)

and balanced power distribution (51% dynamic, 49% static), making it suitable for FPGA/ASIC implementations. However, timing fixes, bit-width adjustments, and rigorous sign-extension checks were critical to ensuring correctness. The architecture's scalability and modularity support extensions to higher bit-widths, while its low-area footprint aligns with constrained embedded systems.

5.1 Scope:

The proposed hybrid multiplier architecture offers significant potential for future enhancements, including **power optimization** through clock gating and operand isolation to reduce dynamic power consumption, **pipelining** to improve throughput for high-frequency applications, and **extended bit-widths** (16/32-bit) to support broader DSP and AI use cases. Additionally, exploration of **emerging technologies** like quantum-dot cellular automata (QCA) or memristor-based implementations could further enhance energy efficiency, while **approximate computing** techniques could be leveraged for error-tolerant applications such as machine learning. With its modular and scalable design, the architecture remains highly adaptable, ensuring relevance in real-time signal processing, AI accelerators, and edge computing devices, effectively bridging the gap between academic research and industrial requirements for high-performance, low-power arithmetic units.

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